

J6/Vayu/TDA2x SoC Automotive PCB Design Rules

Prepared By: Bill McCracken

Date/Rev:

May 27, 2015 – Minor text updates

Added “Min Land Size Derivation” to Reference section

May 18, 2015 – Changed TDA3x references to TDA2x; Updated IPC Classification slides to align with latest IPC-2221, RevB standard; Added PCB Design Tradeoff & J6 23x23, ABC package drawing

May 15, 2015 – Increased BGA land pad dia from 0.356 to 0.4mm to align for best solder & mechanical reliability, updated IPC background slide

Dec 02, 2014 – Added Ref Design slides, clarified slide titles & added CDDS link for Ref PCB

Aug 15, 2014 – Added slide with Reference Design CDDS links

April 09, 2014 – Fixed typos on Class-3 slides

April 08, 2014 – Added IPC Class-2 & Class-3 PCB Design Parameter tables & supporting diagrams; Clarified J6 8-Layer Ref PCB Design Parameter & Diagrams

Dec 16, 2013 – Updated Via size to 18/8mils (Ring/Drill) per feedback from Via Systems for

TI Confidential – NDA Restrictions

Class 2 PCB.



Reference Design

- Design Optimization Study
 - OrCAD SCH & Allegro PCB source files provide a starting point
 - Verified SoC Schematic Symbol
 - IPC-Class 2 PCB design parameters
 - Through-hole vias, PCB thickness & conductor clearance
 - Reduces PCB manufacturing costs & improves reliability
 - 100% signal & power breakout
 - 23x23 Via Channel BGA
 - Total of 8 layers
 - DDR3 Matched Group Routing examples for dual EMIFs
 - Power Integrity Modeling using “3D” CAD Tool (Sentinel PSI – v13.1.1) enables
 - Optimized decoupling capacitor schemes per power domain
 - Reducing number of capacitors & saving PCB area
 - Robust Power Distribution Network
 - PCB routing examples per power domain
 - Reduced decoupling capacitor trace inductance
 - Minimizes impedance vs freq, thereby reducing transient/switching noise levels
 - Enables low AVS voltages for OPPs thereby minimizing junction temps while achieving optimal processor performance

IPC Standards for PCB Design

- IPC is “Association Connecting Electronics Industries”
 - “The global trade association serving the printed board and electronics assembly industries, their customers and suppliers.”
- IPC-2221 “Generic Standard on Printed Board Design”
 - History
 - Revision B, Nov. 2012
 - Revision A, May. 2003
 - Amend, Jan 2000
 - Original, Nov 1998
 - Scope
 - “Establish the generic requirements for the design of organic printed boards...”
 - Purpose
 - “Establish design principles and recommendations” for producing PCB designs across 3 end product classifications and 3 levels of PCB producibility.

IPC Standards for PCB Design

– Performance Classifications

- 3 different classifications based upon end product use
- All new definitions per updated IPC-2221, RevB

Class 1 General Electronic Products – Includes limited life products suitable for applications where the requirement is function of the completed product.

Class 2 Dedicated Service Electronic Products – Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical.

Class 3 High Reliability Electronic Products – Includes products where continued high performance or performance-on-demand is critical, product downtime cannot be tolerated, and the product must function when required.

– Producibility Levels

- 3 different levels to communicate the degree of difficulty of a feature between design and fabrication/assembly facilities.
- Only Level C is new per updated IPC-2221, RevB

Level A General Design Producibility-Preferred

Level B Moderate Design Producibility-Standard

Level C Least Design Producibility-Reduced

PCB Design Parameter Tradeoffs

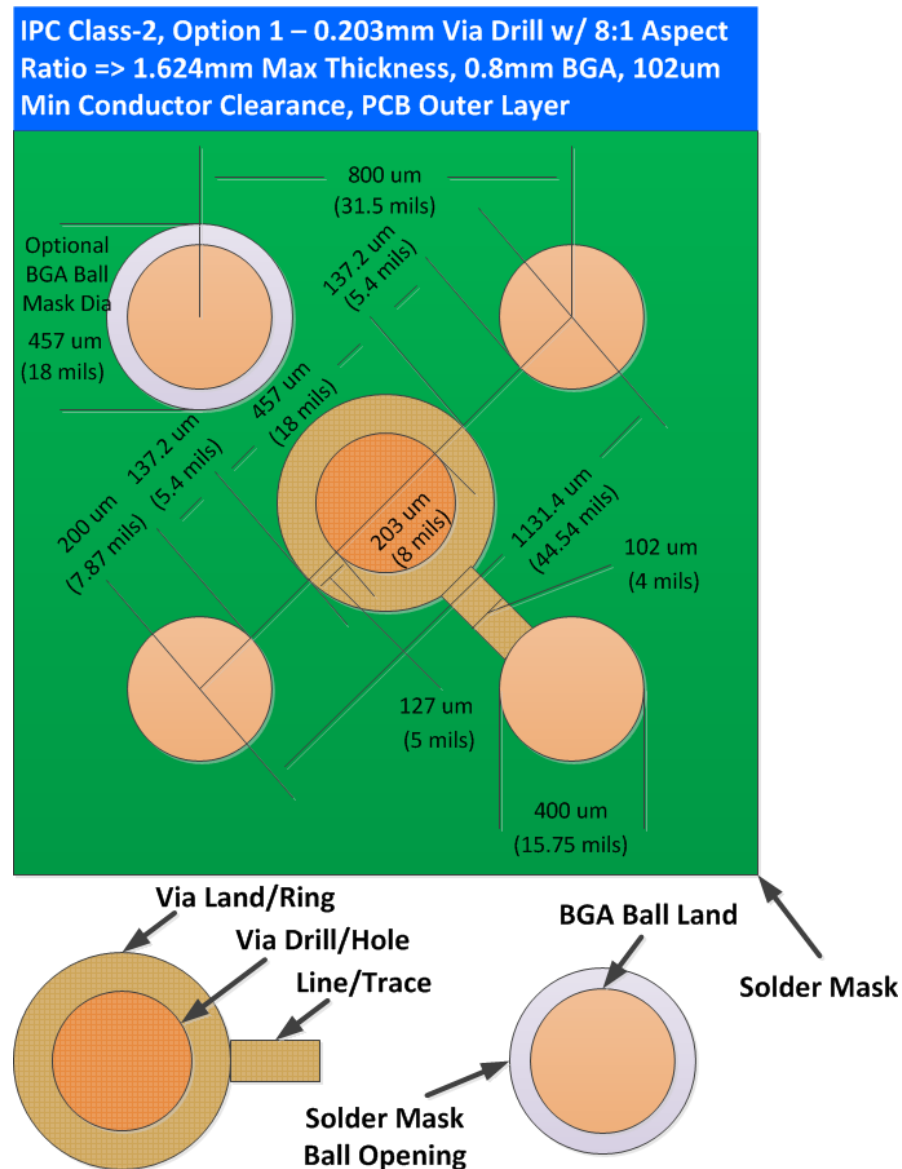
- Determining a set of PCB design parameters should begin with understanding the End Product uses, environment & lifetime goals along with PCB producibility concerns
- TI recommends starting with a BGA PCB pad size equal to the components substrate pad size & solder ball diameter
 - PCB pad = Substrate pad recommendation offers:
 - Reliable solder joints over thermal cycling
 - Robustness under mechanical stresses
 - Compatible with PCB fabrication vendor capabilities
- Customer must select final PCB design parameters that meet their End Product needs and are typically a tradeoff between:
 - PCB fabrication cost
 - Reliability under stress
 - Ease of routing
 - Layer count, Via type & size, Trace Width & Space, Total Number of Interface & Controlled Impedance Signals, Signal & Power Integrity

J6 Auto PCB Design Rules for IPC Class-2; Option 1 – 1.624mm Max Thickness, 102um Conductor Clearance

Items	IPC Class-2, 8-Layer Ref PCB [mm] (mil = 1/1000inch)
BGA Ball Pitch	0.800 (31.5)
BGA Ball Pad/Land Diameter (Dia)	0.400 (15.75)
BGA Ball Solder Mask to Pad Space (solder resist – conductor)	0.1085 to 0 (4.0 to 0) {where 0 = solder mask defined pad}
Through-Hole (TH) Via, Drill-Hole Dia	0.203 (8.0)
Max PCB Thickness = Max Aspect Ratio * TH Via Dia (Volume PCB production desires max Aspect Ratio = 8:1)	1.624 (64.0)
TH Via, Pad/Land Dia, min (IPC Class 2 requires Min Via Land Dia = 10mil + Drill Dia)	0.457 (18.0)
TH Via, Annular Ring Width	0.127 (5.0)
TH Via, Hole – Hole Pitch, min	0.559 (22.0)
Etch/Line Width, min	0.102 (4.0)
Conductor to Conductor Space, min (Conductor = any Cu surface, i.e. Etch, Pad, Via, Plane...)	0.102 (4.0)
Conductor to Drill-Hole Space, min	0.229 (9.0)

TI Confidential – NDA Restrictions

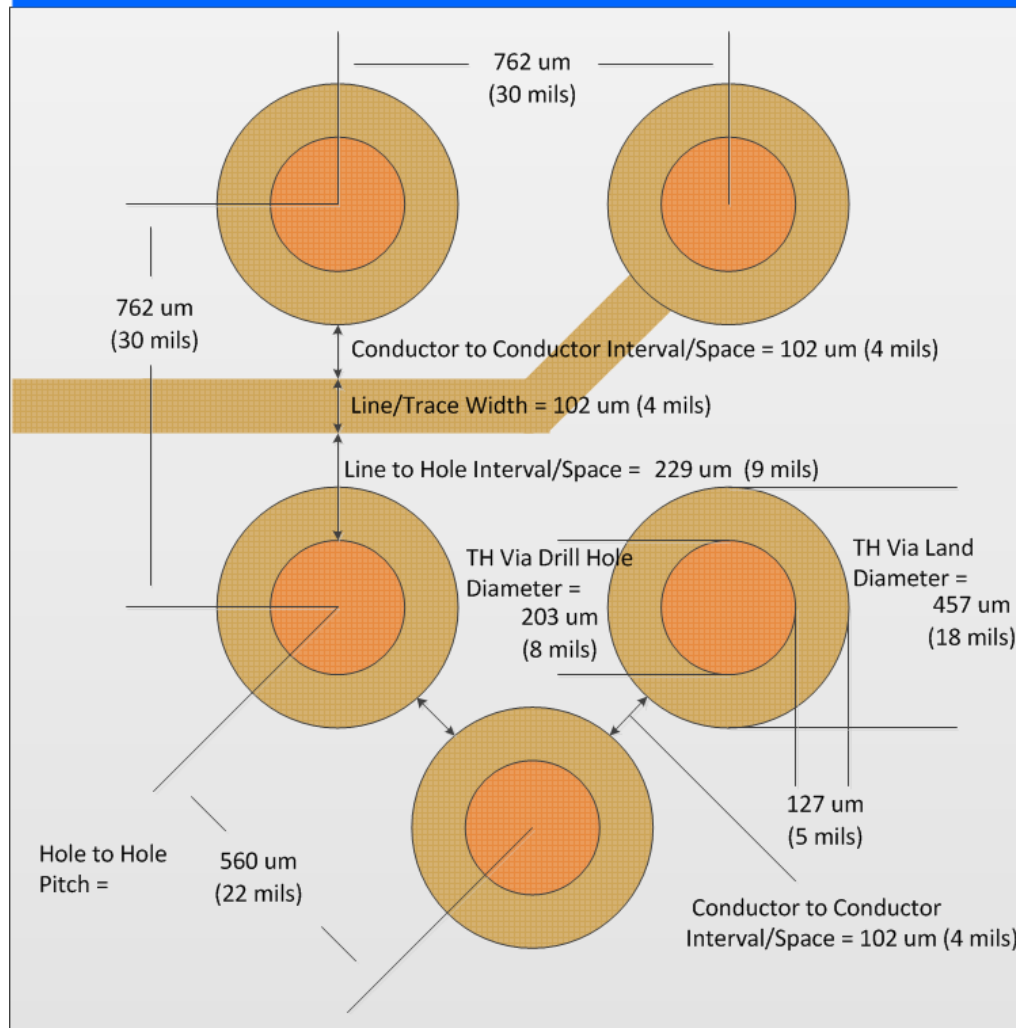
J6 Auto – SoC Footprint/Land Pattern Breakout



TI Confidential – NDA Restrictions

J6 Auto – Routing & Via Placement Minimums

IPC Class-2, Option 1 – 0.203mm Via Drill w/ 8:1 Aspect Ratio => 1.624mm
Max Thickness, 0.8mm BGA Pitch, 102um Trace Width & Min Conductor
Clearance, Via Placement & Routing Minimums

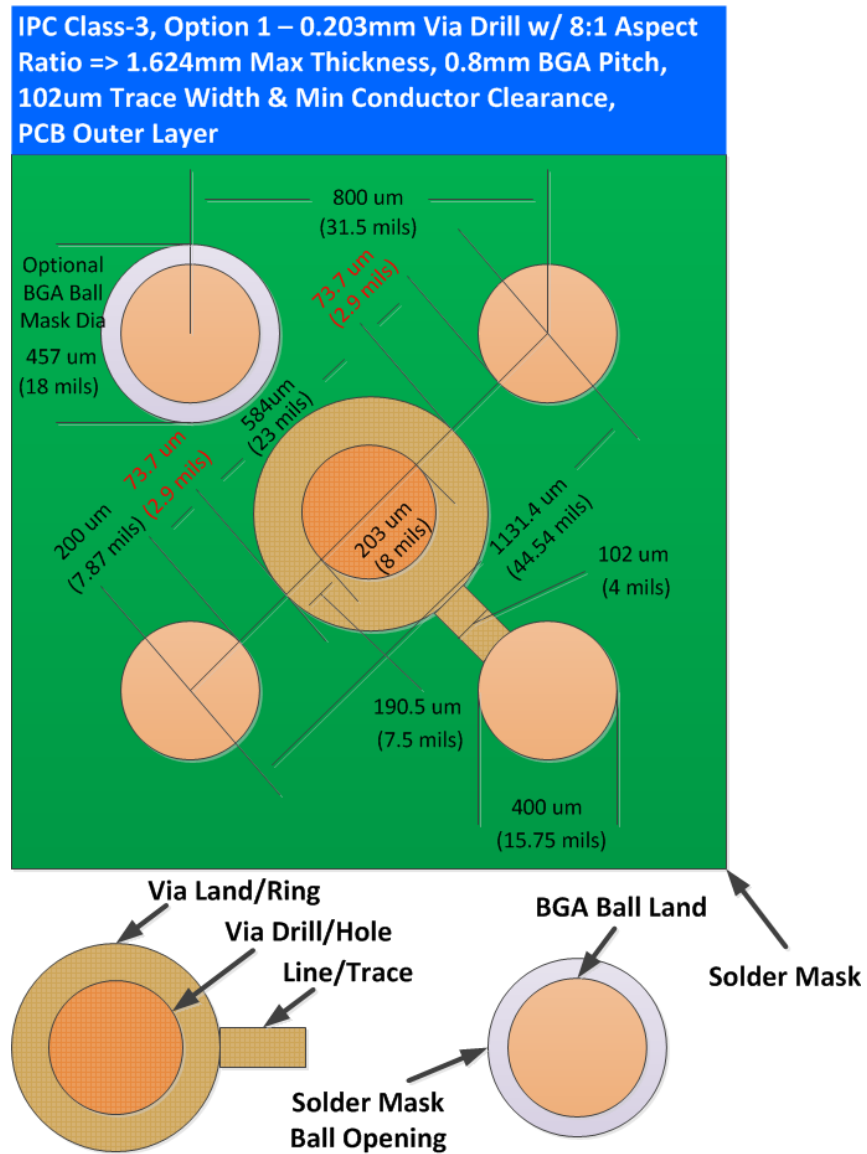


TI Confidential – NDA Restrictions

J6 Auto PCB Design Rules, IPC Class-3; Option 1 – 1.624mm Max Thickness, 96um Conductor Clearance

Items	IPC Class-3, Option 1 [mm] (mil = 1/1000inch)
BGA Ball Pitch	0.800 (0.0315)
BGA Ball Pad/Land Diameter (Dia)	0.400 (0.01575)
BGA Ball Solder Mask to Pad Space (solder resist – conductor)	0.1085 to 0 (4.0 to 0) {where 0 = solder mask defined pad}
Through-Hole (TH) Via, Drill-Hole Dia	0.203 (8.0)
Max PCB Thickness = Aspect Ratio * TH Via Drill Dia (Volume PCB production desires an Aspect Ratio = 8:1)	1.624 (64.0)
TH Via, Pad/Land Dia (IPC Class 3 requires min Via Ring Dia = 15mil + Drill Dia)	0.584 (23.0) (Blue font = Class 3 changes)
TH Via, Annular Ring Width	0.1905 (7.5)
TH Via, Hole – Hole Pitch, min	0.559 (22.0)
Etch/Line Width, min	0.102 (4.0)
Conductor to Conductor Space, min (Conductor = any Cu surface, i.e. Etch, Pad, Via, Plane...)	Desired = 0.102 (4.0) Actual = 0.0737 (2.9)
Conductor to Drill-Hole Space, min	0.292 (11.5)

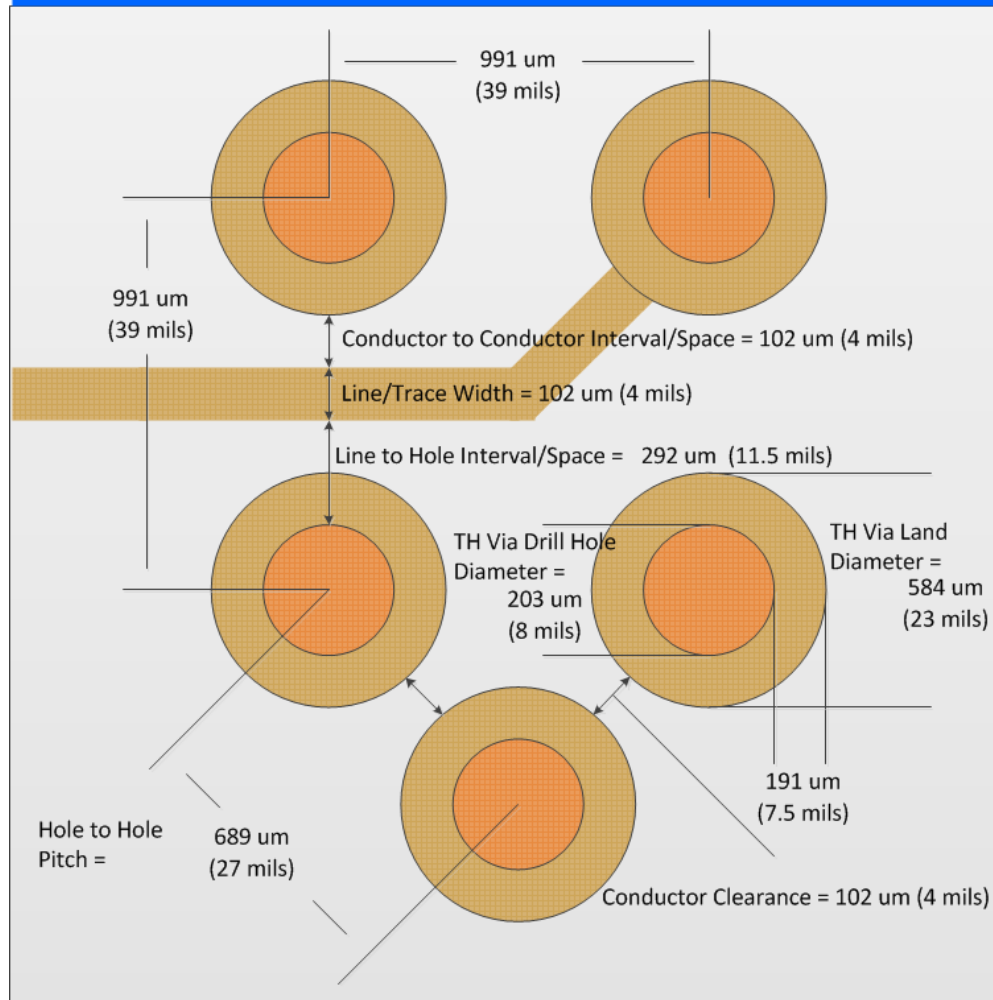
J6 Auto – SoC Footprint/Land Pattern Breakout



TI Confidential – NDA Restrictions

J6 Auto – Routing & Via Placement Minimums

IPC Class-3, Option 1 – 0.203mm Via Drill w/ 8:1 Aspect Ratio => 1.624mm
Max Thickness, 0.8mm BGA, 102um Trace Width & Min Conductor
Clearance, 23/8mil Via Dia/Drill Placement & Routing Minimums

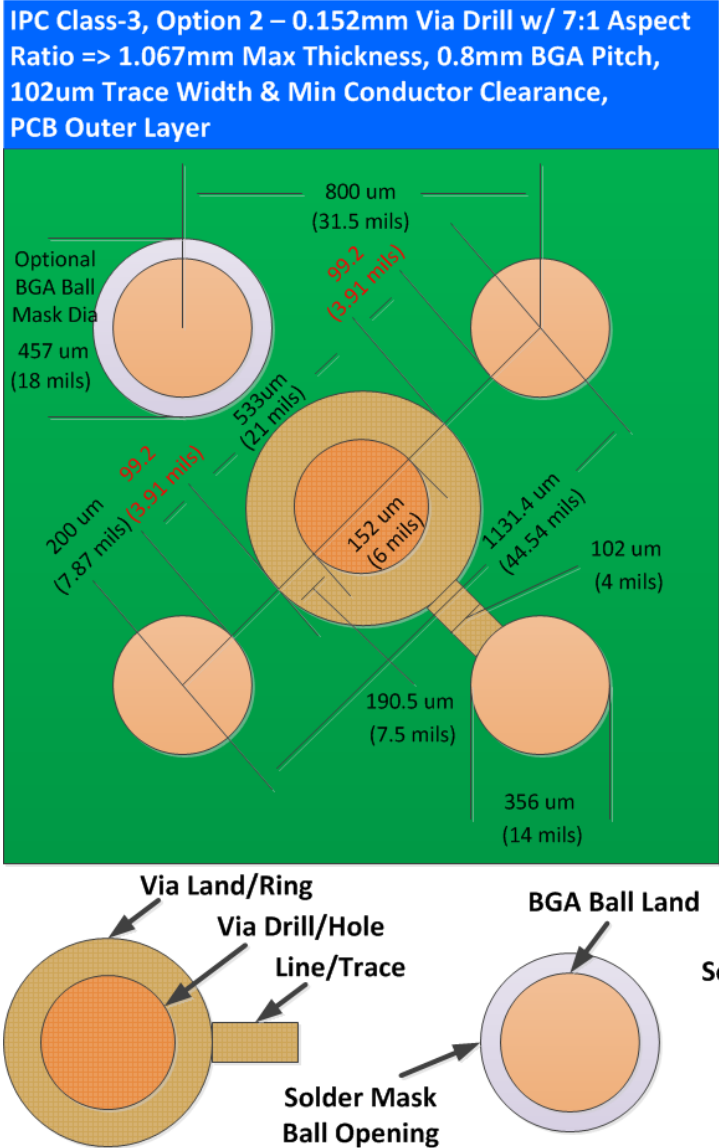


TI Confidential – NDA Restrictions

J6 Auto PCB Design Rules, IPC Class-3, Option 2 – 1.067mm Max Thickness, 121um Conductor Clearance

Items	IPC Class-3, Option 2 [mm] (mil = 1/1000inch)
BGA Ball Pitch	0.800 (0.0315)
BGA Ball Pad/Land Diameter (Dia)	0.400 (0.01575)
BGA Ball Solder Mask to Pad Space (solder resist – conductor)	0.1085 to 0 (4.0 to 0) {where 0 = solder mask defined pad}
Through-Hole (TH) Via, Drill-Hole Dia	0.152 (6.0) (Blue font = Class 3, Opt 2 changes)
Max PCB Thickness = Aspect Ratio * TH Via Drill Dia (Volume PCB production desires an Aspect Ratio = 8:1)	1.067 (42.0)
TH Via, Pad/Land Dia (IPC Class 3 requires min Via Ring Dia = 15mil + Drill Dia)	0.533 (21.0)
TH Via, Annular Ring Width	0.191 (7.5)
TH Via, Hole – Hole Pitch, min	0.559 (22.0)
Etch/Line Width, min	0.102 (4.0)
Conductor to Conductor Space, min (Conductor = any Cu surface, i.e. Etch, Pad, Via, Plane...)	Desired = 0.102 (4.0) Actual = 0.0992 (3.91)
Conductor to Drill-Hole Space, min	0.292 (11.5)

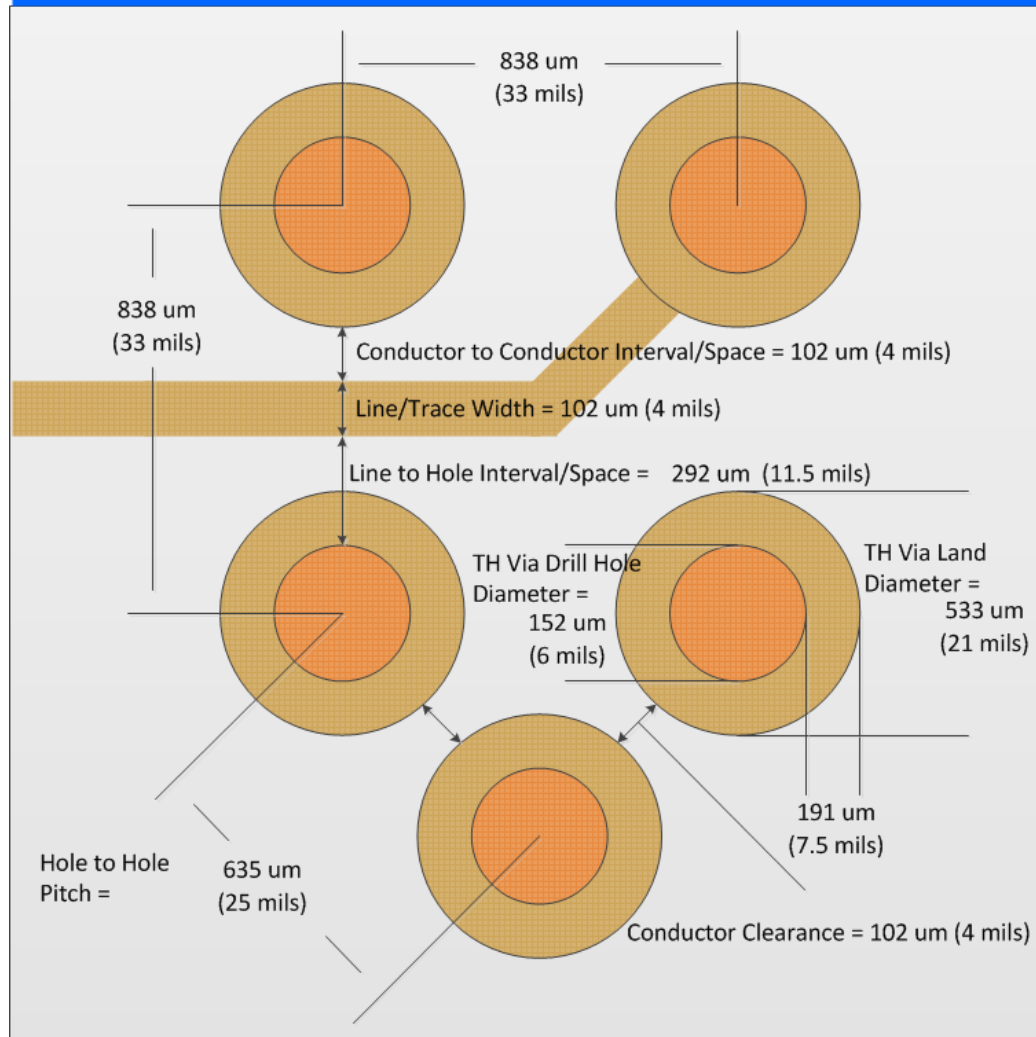
J6 Auto – SoC Footprint/Land Pattern Breakout



TI Confidential – NDA Restrictions

J6 Auto – Routing & Via Placement Minimums

IPC Class-3, Option 2 – 0.152mm Via Drill w/ 7:1 Aspect Ratio => 1.067mm
Max Thickness, 0.8mm BGA, 102um Min Conductor Clearance,
21/6mil Via Dia/Drill Placement & Routing Minimums



TI Confidential – NDA Restrictions

Actual J6/TDA2x Reference PCB Design

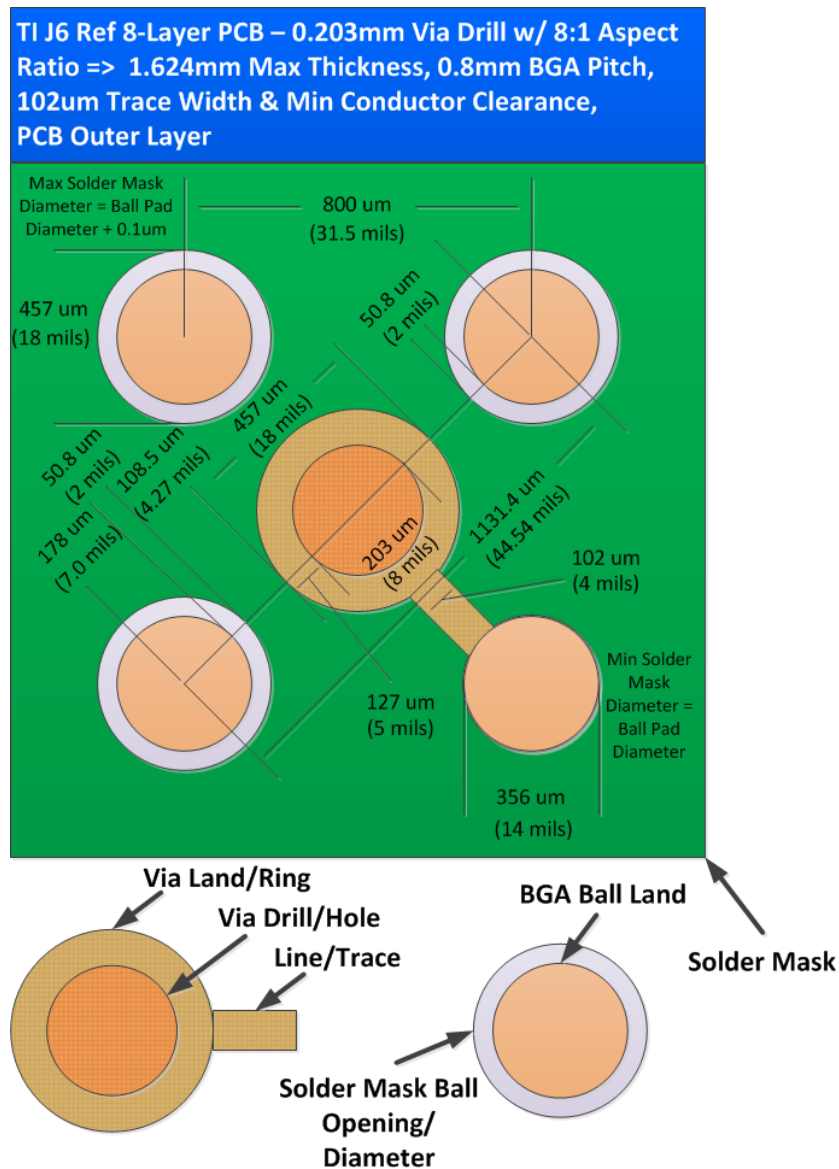
- Two different via pad & drill sizes were used based upon PCB location
 - Underneath SoC BGA footprint
 - Via Pad/Land diameter = 0.457mm / 18mil
 - Via Drill diameter = 0.203mm / 8mil
 - Outside SoC BGA footprint
 - Via Pad/Land diameter = 0.508mm / 20mil
 - Via Drill diameter = 0.254mm / 10mil
 - Minimizes quantity of 0.203mm/8mil drill holes
 - Used only where they are needed to achieve 100% breakout
 - Potentially improves PCB yield loss since majority of drills will be 0.254mm / 10mil
 - Potentially reducing PCB costs

J6 Auto Ref PCB Design Rules (under SoC) = IPC Class-2; Option 1, 1.624mm Max Thickness, 102um Conductor Clearance

Items	IPC Class-2, 8-Layer Ref PCB [mm] (mil = 1/1000inch)
BGA Ball Pitch	0.800 (0.0315)
BGA Ball Pad/Land Diameter (Dia)	0.356 (0.014)
BGA Ball Solder Mask to Pad Space (solder resist – conductor)	0.1085 to 0 (4.0 to 0) {where 0 = solder mask defined pad}
Through-Hole (TH) Via, Drill-Hole Dia	0.203 (8.0)
Max PCB Thickness = Aspect Ratio * TH Via Drill Dia (Volume PCB production desires an Aspect Ratio = 8:1)	1.624 (64.0)
TH Via, Pad/Land Dia (IPC Class 2 requires min Via Ring Dia = 10mil + Drill Dia)	0.457 (18.0)
TH Via, Annular Ring Width	0.127 (5.0)
TH Via, Hole – Hole Pitch, min	0.559 (22.0)
Etch/Line Width, min	0.102 (4.0)
Conductor to Conductor Space, min (Conductor = any Cu surface, i.e. Etch, Pad, Via, Plane...)	0.102 (4.0)
Conductor to Drill-Hole Space, min	0.229 (9.0)

TI Confidential – NDA Restrictions

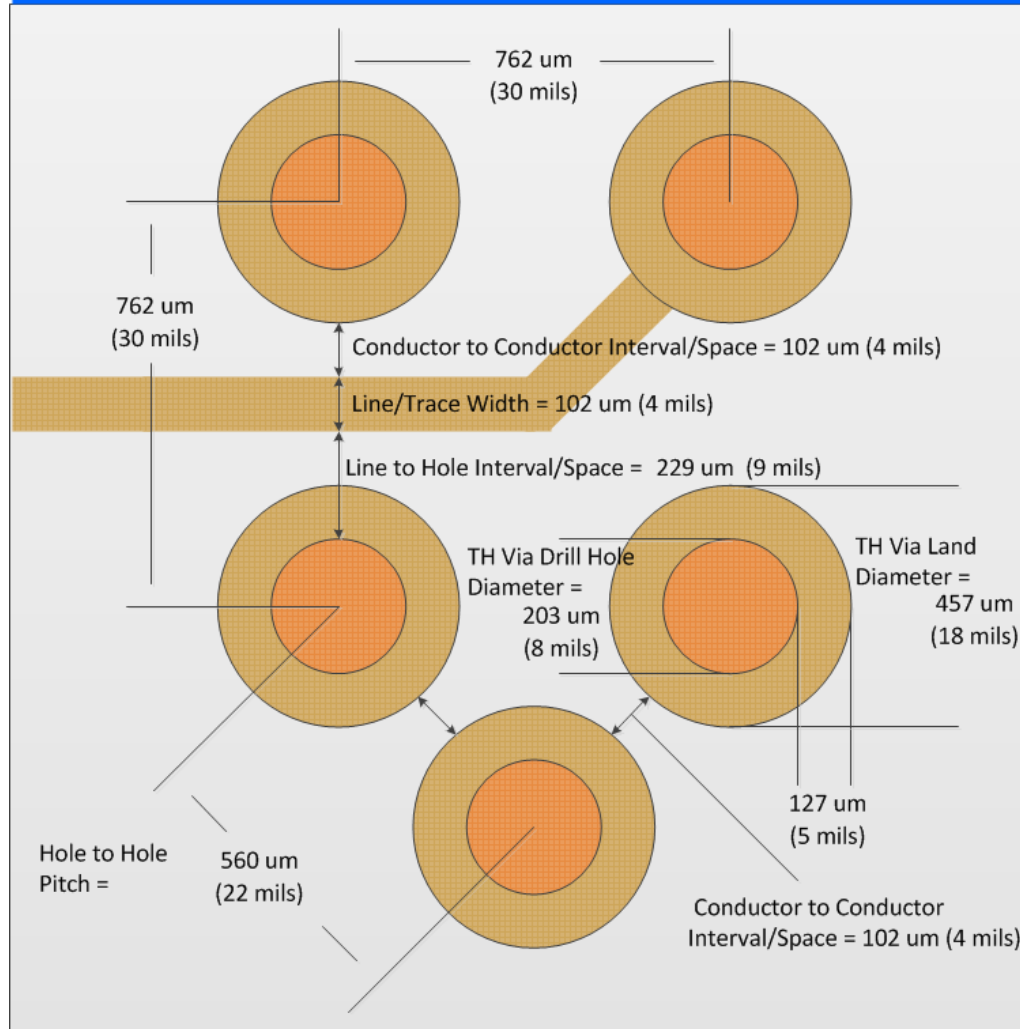
J6 Auto Ref – SoC Footprint/Land Pattern Breakout



TI Confidential – NDA Restrictions

J6 Auto Ref – Routing & Via Placement Minimums

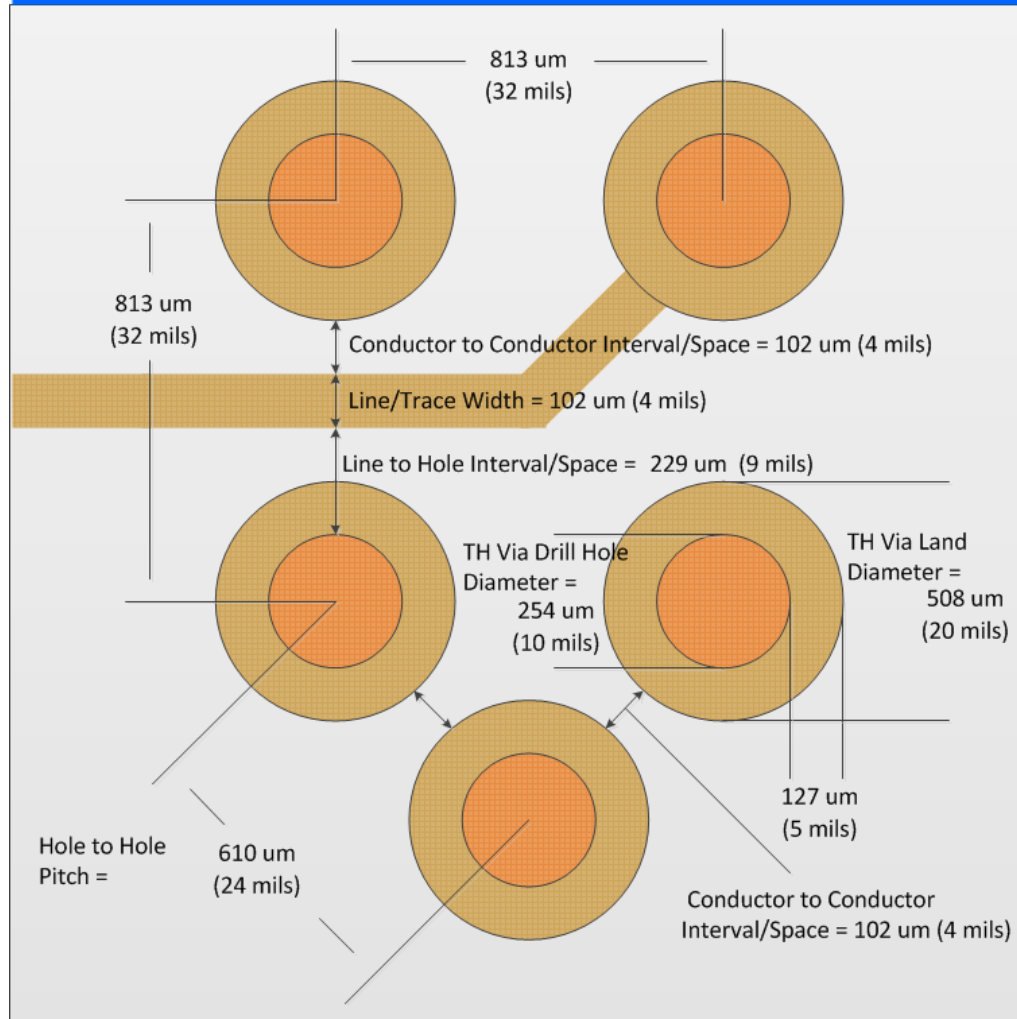
TI J6 Ref 8-Layer PCB – 0.203mm Via Drill w/ 8:1 Aspect Ratio =>
1.624mm Max Thickness, 0.8mm BGA Pitch, 102um Trace Width & Min
Conductor Clearance, 18/8mil Via Dia/Drill Placement & Routing Mins,
Under BGA



TI Confidential – NDA Restrictions

J6 Auto Ref – Routing & Via Placement Minimums

TI J6 Ref 8-Layer PCB – 0.203mm Via Drill w/ 8:1 Aspect Ratio =>
1.624mm Max Thickness, 0.8mm BGA Pitch, 102um Trace Width & Min
Conductor Clearance, 20/10mil Via Ring/Drill Routing Minimums,
Outside BGA



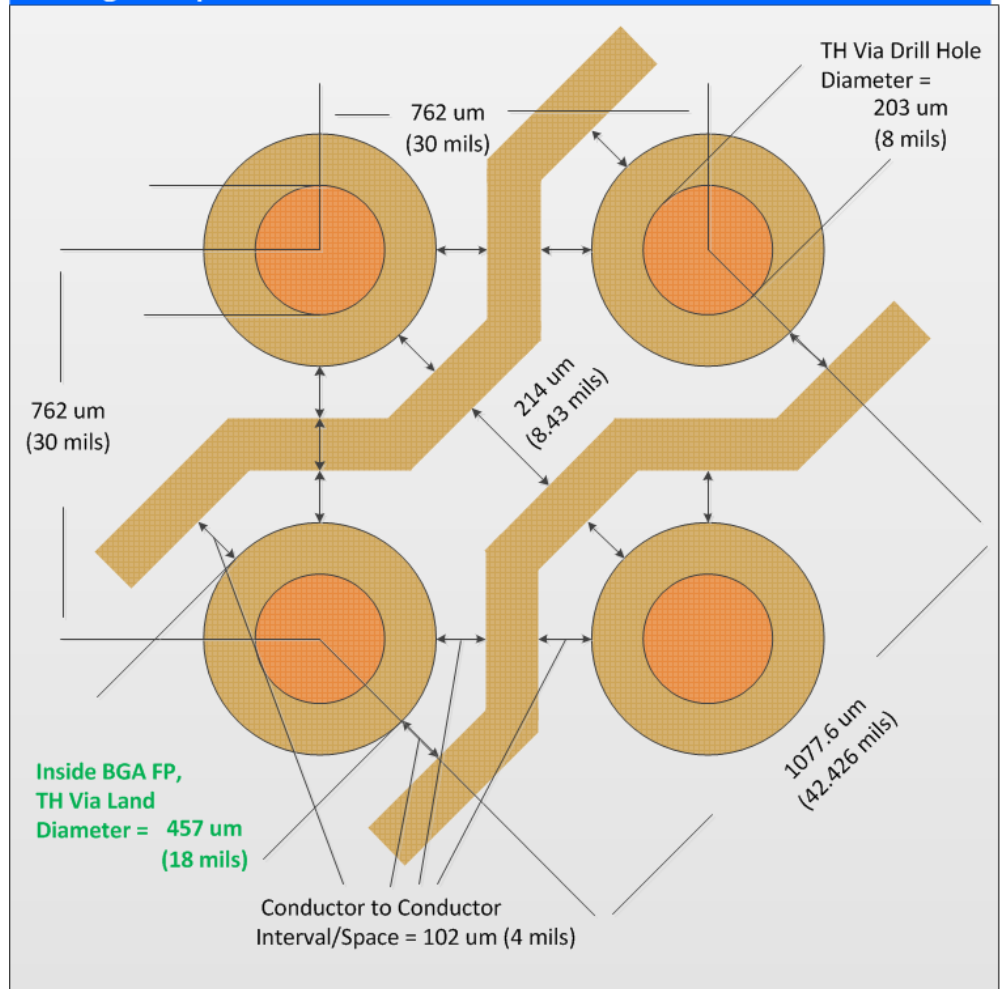
TI Confidential – NDA Restrictions

J6 Auto Ref – Routing & Via Placement for DDR3 Breakout

Snap-shot from J6 Ref PCB



TI J6 Ref 8-Layer PCB – 0.203mm Via Drill w/ 8:1 Aspect Ratio => 1.624mm Max Thickness, 0.8mm BGA Pitch, 102um Trace Width & Min Conductor Clearance, 18/8mil Via Ring/Drill Routing Minimums, Routing Example Under BGA



TI Confidential – NDA Restrictions

J6 Auto Ref - PCB Stackup

PCB Stack-up Details

DDI Sales Corp
A Subsidiary of Viasystems
8150 Sheppard Ave E
Toronto, ON, M1B 5K2

Job Name : QCG-SPECTRUM_106407-01E5

Customer : QCG

Part Num : 106407-01

Part Rev : E

Engineer : David Gorden



Layer	Calc Thickness	Primary Stack	Description	Dk / Df
Layer - 1	0.0005 0.0020		Taiyo 4000-BN	4.71 / 0.0330
Layer - 2	0.0029 0.0006	1080	1/2oz Mix (Std Plt)	4.12 / 0.0210
Layer - 3	0.0050 0.0006	0.0050 (1-1652)	370H	4.64 / 0.0180
Layer - 4	0.0060 0.0025	1080 2113	1/2oz Mix	4.33 / 0.0210
Layer - 5	0.0210 0.0025	0.021 (5-2116)	370H	4.51 / 0.0210
Layer - 6	0.0061 0.0006	2113 1080	2oz P/G	4.32 / 0.0210
Layer - 7	0.0050 0.0006	0.0050 (1-1652)	370H	4.64 / 0.0180
Layer - 8	0.0029 0.0020 0.0005	1080	1/2oz P/G	4.12 / 0.0210
			1/2oz Mix (Std Plt)	4.71 / 0.0330
			Taiyo 4000-BN	

Materials: Isola 370H High-Tg FR4

Requirement	Req. Thickness	Tol +	Tol -	Calc Thick
Incl. Plating & Mask	0.0620	0.0062	0.0062	0.0613
Incl. Mask over Laminate	0.0580	0.0058	0.0058	0.0573
Incl. Plating	0.0610	0.0061	0.0061	0.0603
After Lamination	0.0582	0.0029	0.0029	0.0575
Over Laminate	0.0570	0.0057	0.0057	0.0563

TI Confidential – NDA Restrictions

21

J6 Auto Ref - PCB Controlled Impedance Plan

Controlled Impedance Details for PCB Stackup PN: 106407-01, Rev E

#	Impedance Type		Layer	Line Width [mm {mils}]	Line Pitch [mm {mils}]	Ref Plane	Impedance Target+/-Tol [ohms]	Model [ohms]	Signal Names
1	Single-Ended Microstrip		L1-Top	0.10795 {0.00425}	NA	L2-Gnd1	50 +/- 5	49.55	DDR3, QSPI
2	Diff-Paired Microstrip		L1-Top	0.10668 {0.0042}	0.2794 {0.011}	L2-Gnd1	90 +/- 9	89.44	USB3 (preferred , top layer routing & connector)
3	Diff-Paired Microstrip		L1-Top	0.1016 {0.004}	0.3556 {0.014}	L2-Gnd1	96 +/- 9.6	95.7	HDMI, SATA, PCIe (preferred , top layer routing & connector)
4	Single-Ended Stripline		L3-Sig1	0.1143 {0.0045}	NA	L2-Gnd1 L4-Pwr1	50 +/- 5	49.54	DDR3, QSPI
5	Diff-Paired Stripline		L3-Sig1	0.12192 {0.0048}	0.2794 {0.011}	L2-Gnd1 L4-Pwr1	90 +/- 9	89.1	
6	Diff-Paired Stripline		L3-Sig1	0.10668 {0.0042}	0.3556 {0.014}	L2-Gnd1 L4-Pwr1	100 +/- 10	99.61	PCIe, SATA

TI Confidential – NDA Restrictions

J6 Auto Ref - PCB Controlled Impedance Plan

Controlled Impedance Details - continued

#	Impedance Type		Layer	Line Width [mm {mils}]	Line Pitch [mm {mils}]	Ref Plane	Impedance Target+/-Tol [ohms]	Model [ohms]	Signal Names
7	Single-Ended Stripline		L6-Sig2	0.1143 {0.0045}	NA	L5-Pwr2 L7-Gnd2	50 +/- 5	49.75	DDR3, QSPI
8	Diff-Paired Stripline		L6-Sig2	0.12192 {0.0048}	0.2794 {0.011}	L5-Pwr2 L7-Gnd2	90 +/- 9	89.36	
9	Diff-Paired Stripline		L6-Sig2	0.10668 {0.0042}	0.3556 {0.014}	L5-Pwr2 L7-Gnd2	100 +/- 10	99.94	PCIe, SATA
10	Single-Ended Microstrip		L8-Bottom	0.10795 {0.00425}	NA	L7-Gnd2	50 +/- 5	49.55	DDR3, QSPI
11	Diff-Paired Microstrip		L8-Bottom	0.10668 {0.0042}	0.2794 {0.011}	L7-Gnd2	90 +/- 9	89.44	USB3 (alternate layer, for bottom-side connector)
12	Diff-Paired Microstrip		L8-Bottom	0.1016 {0.004}	0.3556 {0.014}	L7-Gnd2	96 +/- 9.6	95.71	HDMI (alternate layer, for bottom-side connector)

TI Confidential – NDA Restrictions

References:

Link to IPC-2221A Generic Standard on PCB

http://sisko.colorado.edu/CRIA/FILES/REFS/Electronics/IPC_2221A.pdf

Link to IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards

<http://222.184.16.210/smt/tzxt/bz/IPC-2222.pdf>

Link to “Design Rules & DFM for High-Speed Design” article from June 2012 issue of *The PCB Magazine*.

http://www.pcbdesign007.com/pages/columns.cgi?clmid=65&artid=85453&_pf=1

Link below explains IPC Class differences in PCB

<http://www.circuitnet.com/experts/86649.shtml>

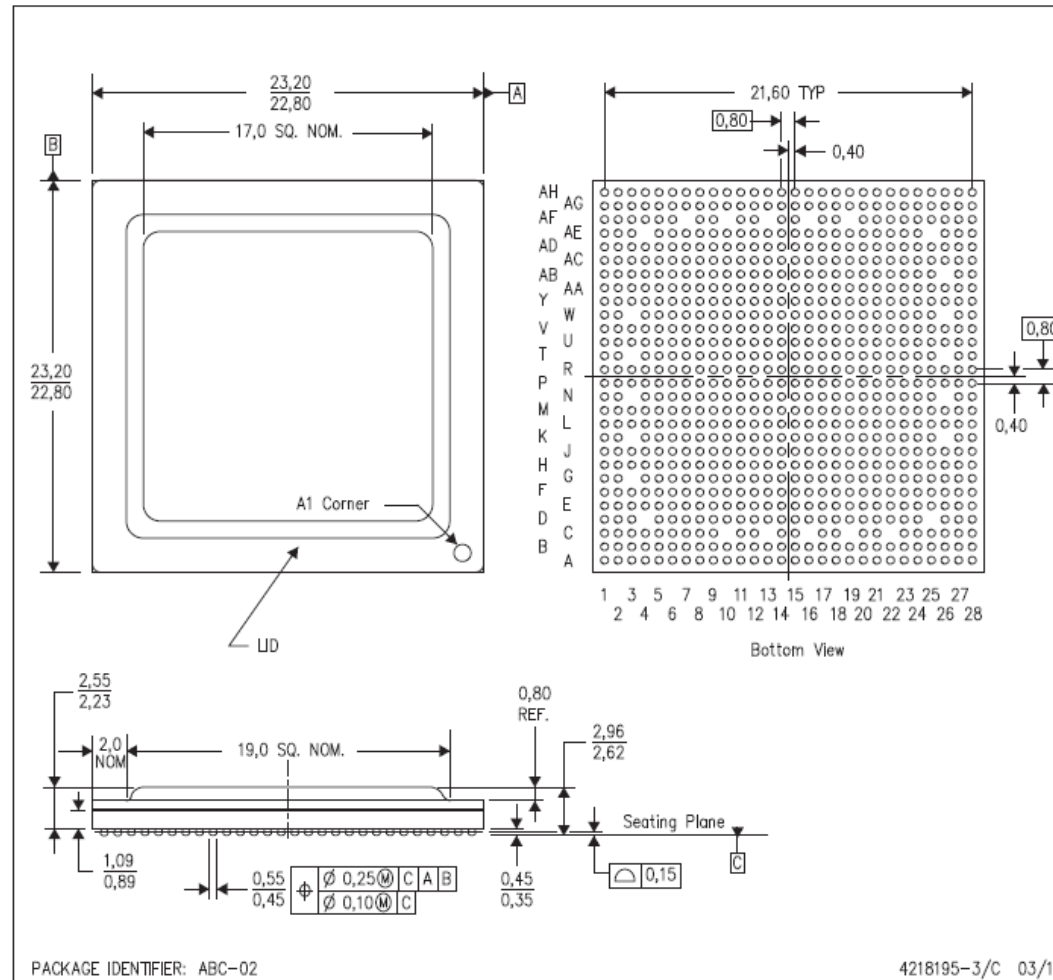
CDDS Link to J6/Vayu/TDA2 Reference PCB Design Source & Support Files

<https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.33317.4164>

J6 23x23, 760-Ball Plastic BGA (ABC package)

ABC (S-PBGA-N760)

PLASTIC BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Thermally enhanced plastic package with lid.
E. Pb-free die bump and solder ball.

“Min Via Land Size” Derivation

- Class3 type PCBs require a min Annular Ring (AR) for all Plated Through-Holes (PTHs) per section 9.1.2 & Figs 9-1 & 9-2, shown below:
- IPC defines the min Land size equation to be:
 - Min Land Size = Drill Size + 2 * Min Annular Ring + Fab Allowance
 - Add 1.968mils [50 um] of margin for each 1oz/sq ft of Cu weight (Table 9-1, Note 1)
 - Add 1.968mils [50 um] of margin for PCB's exceeding 8-layers (Table 9-1, Note 2)
 - For Class3 PCBs with a Drill Size = 8mils, External Land (Table 9-2) & “Standard” (Level B) Manufacturing (Table 9-1)
 - Min Land Size = $8 + 2 * 1.968\text{mils} + 9.84 = 21.776\text{mils}$ [0.5785mm]
 - Min Land Size for PCBs over 8-layers or Cu weight > 1.0 oz = 23.744mils [0.6031mm]
 - Hence “Industry Rule of Thumb” for Class3 PCBs (All Cu < 1 oz/sqft & Layers <= 8):
 - Min Land Size = Drill Size + 15mils [0.381mm] (some PCBs request “+ 14mils”)

“Min Via Land Size” Derivation

- Class1 and 2 type PCBs are allowed to have a “partial hole breakouts” per section 9.1.2 & Appendix B, Fig B.10-1 (“Tangent Breakout”) shown below:
 - Essentially, “no min Annular Ring” is acceptable for Class 1 & 2 products
- IPC defines the min Land size equation to be:
 - Min Land Size = Drill Size + 2 * Min Annular Ring + Fab Allowance
 - Add 1.968mils [50 um] of margin for each 1oz/sq ft of Cu weight (Table 9-1, Note 1)
 - Add 1.968mils [50 um] of margin for PCB’s exceeding 8-layers (Table 9-1, Note 2)
 - For Class3 PCBs with a Drill Size = 8mils, External Land (Table 9-2) & “Standard” (Level B) Manufacturing (Table 9-1)
 - Min Land Size with “No AR” = $8 + 2 * 0\text{mils} + 9.84 = 17.84\text{mils}$ [0.4531mm]
 - Hence “Industry Rule of Thumb” for Class2 PCBs (All Cu < 1 oz/sqft & Layers <= 8):
 - Min Land Size = Drill Size + 10mils [0.381mm]

“Min Via Land Size” Derivation

- IPC 2221 spec, sections 9.1.1 & 9.1.2 as shown below:

9.1.1 Land Requirements All lands and annular rings shall be maximized wherever feasible, consistent with good design practice and electrical clearance requirements. When clearances are provided for unsupported holes in the place of external lands these shall meet the minimum edge spacing requirement. Failure to provide adequate land or clearance for unsupported holes will result in excessive rejections due to the common “50-percent” rule for “nicks” and “crazing.” Printed boards constructed with laminates prone to crazing such as polyimide but including other “brittle” materials will benefit from the use of oversized external lands and clearances. To meet the annular ring requirements specified in section 9.1.2, the minimum land surrounding a supported, or unsupported, hole shall be determined by the following. The worst-case land-to-hole relationship is established by the equation:

Land size, minimum = $a + 2b + c$

where:

a = Maximum diameter of the finished hole.

Note: For external layers, the requirement is the maximum diameter of the finished hole. For internal layers, the drill hole diameter is used.

b = Minimum annular ring requirements (see Section 9.1.2).

Note: Etchback, when required, shall be included within the calculation.*

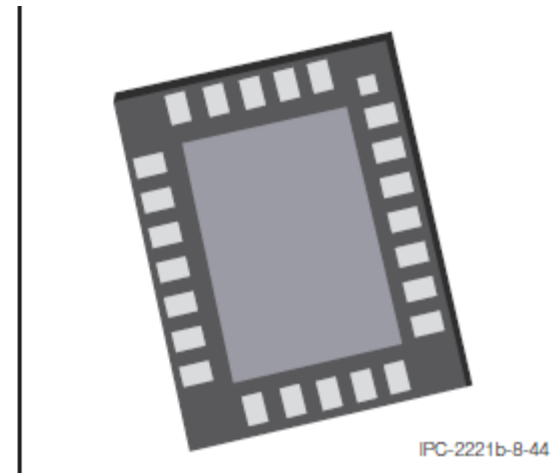


Figure 8-44 Pullback Quad Flat No Lead (PQFN) Construction

“Min Via Land Size” Derivation

IPC-2221B

November 2012

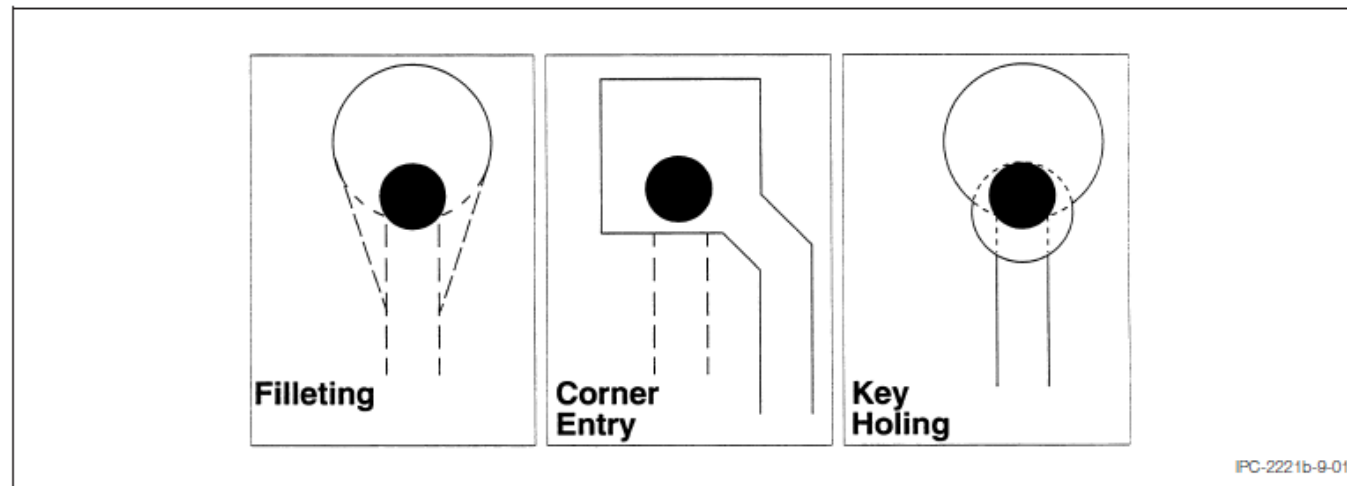


Figure 9-1 Examples of Modified Land Shapes

c = A standard fabrication allowance, detailed in Table 9-1, which considers production master tooling and process variations required to fabricate printed boards.

Note: Refer to the specific sectional design standard for additional processing allowance.

*Etchback, when required, will reduce the insulation area that supports the internal land. The minimum annular ring considered in the design **shall not** be less than the maximum etchback allowed.

Table 9-1 Minimum Standard Fabrication Allowance for Interconnection Lands

Level A	Level B	Level C
0.4 mm [0.016 in]	0.25 mm [0.00984 in]	0.2 mm [0.0079 in]

Note 1. For copper weights greater than 1oz/sq.ft., add 50 μ m [1,968 μ in] minimum to the fabrication allowance for each additional oz/sq. ft. of copper used.

Note 2. For more than 8 layers add 50 μ m [1,968 μ in].

Note 3. See 1.6.3 for definition of Levels A, B and C.

Note 4. Refer to IPC-2226 for allowances for HDI and micro-BGA substrates.

“Min Via Land Size” Derivation

9.1.2 Annular Ring Requirements An annular ring shall be required for all PTHs in Class 3 designs. The performance specifications for Class 1 and Class 2 products may allow partial hole breakouts. The design for these products should take into consideration that breakout is undesirable and the design should require adequate hole and land size so that breakout does not appear in the finished product. Landless holes or holes with partial circumscribing lands shall only be used when approved by the acquiring activity prior to the start of the design process and require conformance specimen that reflect the approach being used.

The minimum annular ring on external layers is the minimum amount of copper (at the narrowest point) between the edge of the hole and the edge of the land after plating of the finished hole (see Figure 9-2). The minimum annular ring on internal layers is the minimum amount of copper (at the narrowest point) between the edge of the drilled hole and the edge of the land after drilling the hole (see Figure 9-3).

9.1.2.1 External Annular Ring The minimum annular ring for unsupported and supported holes shall be in accordance with Table 9-2 and Figure 9-2.

9.1.2.2 Internal Annular Ring The minimum annular ring for internal lands on multilayer and metal core printed boards shall be in accordance with Table 9-2 and Figure 9-3. Etchback, when required, will reduce the insulation supporting the annular ring of internal lands. The minimum annular ring considered in the design shall be not less than the maximum etchback allowed.

“Min Via Land Size” Derivation

November 2012

IPC-2221B

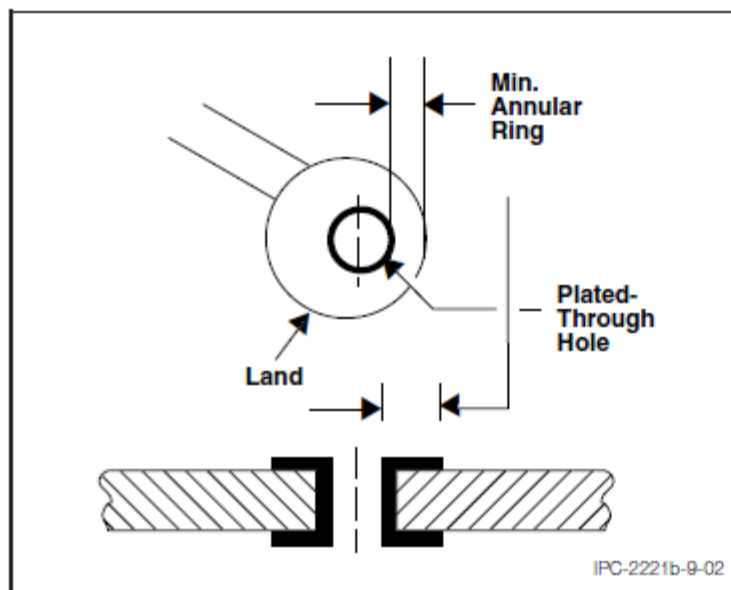


Figure 9-2 External Annular Ring

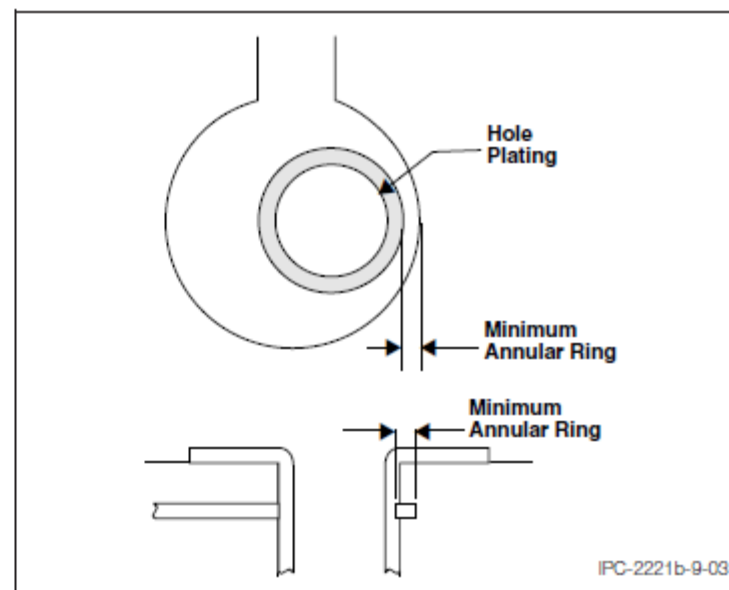


Figure 9-3 Internal Annular Ring

Table 9-2 Annular Rings (Minimum)

Annular Ring	Class 1, 2 and 3
Internal Supported	25.0 μm [984 μin]
External Supported	50.0 μm [1,968 μin]
External Unsupported ¹	0.150 mm [0.00591 in]

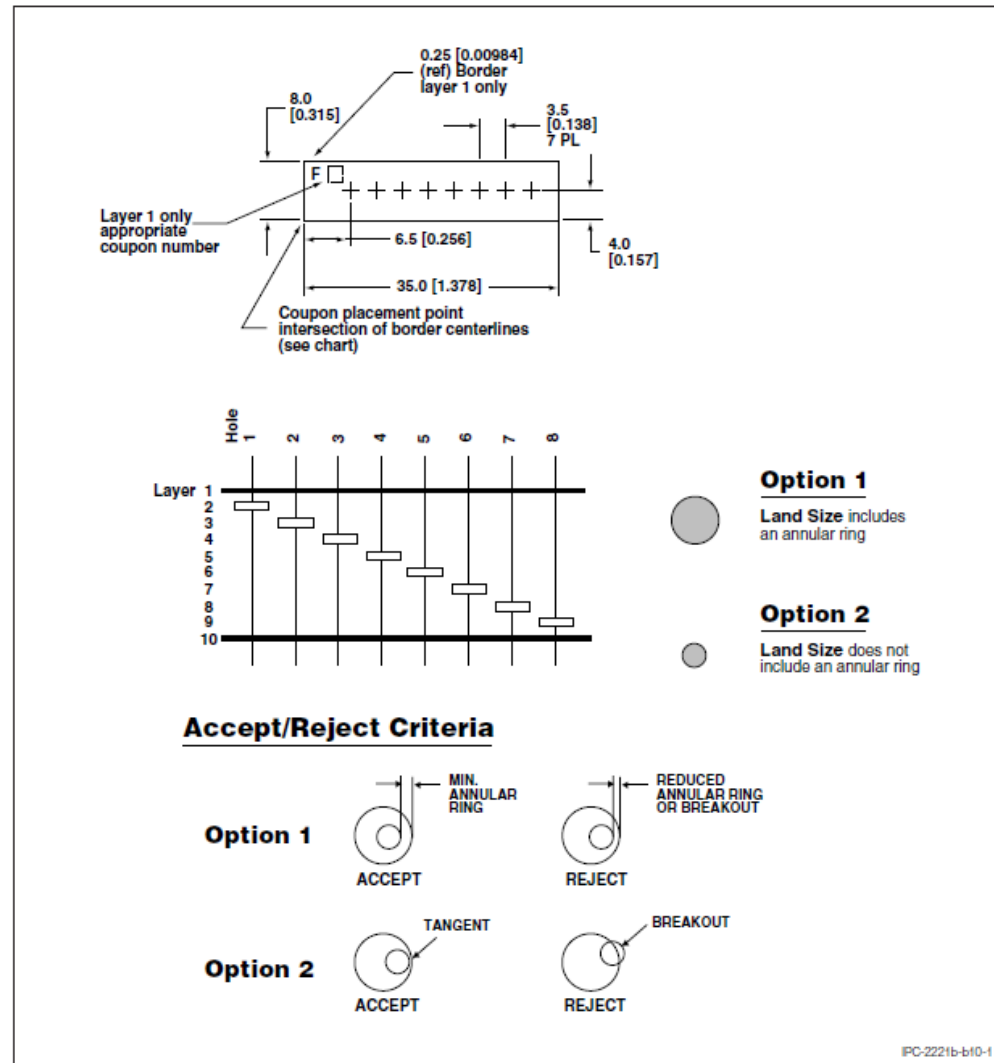
Note 1. The annular ring value for unsupported holes is greater to provide for larger external lands minimizing the loss or damage of pads during processing (drilling, etc.). Printed boards constructed with laminates with low peel strength (e.g., polyimides, etc.) will benefit from the use of oversized external lands.

“Min Via Land Size” Derivation (cont’d)

November 2012

IPC-2221B

- IPC2221 spec, Appendix B, Registration Coupons
 - Purpose: Layer-to-Layer registration and annular ring evaluation without micro-section (e.g. x-Ray)



TI Confidential – NDA Restrictions

32